SECTION 2.3

ELECTRICAL FUNCTION & PERFORMANCE

2.3 ELECTRICAL FUNCTION TEST REQUIREMENTS

The following paragraphs describe the required electrical functional and performance tests that verify the payload's operation before, during, and after environmental testing. These tests along with all other calibrations, functional/performance tests, measurements/ demonstrations, alignments (and alignment verifications), end-to-end tests, simulations, etc., that are part of the overall verification program shall be described in the System Performance Verification Plan.

2.3.1 Electrical Interface Tests

Before the integration of an assembly, component, or subsystem into the next higher hardware assembly, electrical interface tests shall be performed to verify that all interface signals are within acceptable limits of applicable performance specifications.

Prior to mating with other hardware, electrical harnessing shall be tested to verify proper characteristics; such as, routing of electrical signals, impedance, isolation, and overall workmanship.

2.3.2 Comprehensive Performance Tests

A comprehensive performance test (CPT) shall be conducted on each hardware element after each stage of assembly: component, subsystem and payload. When environmental testing is performed at a given level of assembly, additional comprehensive performance tests shall be conducted during the hot and cold extremes of the temperature or thermal-vacuum test for both maximum and minimum input voltage, and at the conclusion of the environmental test sequence, as well as at other times prescribed in the verification plan, specification, and procedures.

The comprehensive performance test shall be a detailed demonstration that the hardware and software meet their performance requirements within allowable tolerances. The test shall demonstrate operation of all redundant circuitry and satisfactory performance in all operational modes within practical limits of cost, schedule, and environmental simulation capabilities. The initial CPT shall serve as a baseline against which the results of all later CPTs can be readily compared.

At the payload level, the comprehensive performance test shall demonstrate that, with the application of known stimuli, the payload will produce the expected responses. At lower levels of assembly, the test shall demonstrate that, when provided with appropriate inputs, internal performance is satisfactory and outputs are within acceptable limits.

2.3.3 Limited Performance Tests

Limited performance tests (LPT) shall be performed before, during, and after environmental tests, as appropriate, in order to demonstrate that functional capability has not been degraded by the tests. The limited tests are also used in cases where comprehensive performance testing is not warranted or not practicable. LPTs shall demonstrate that the performance of selected hardware and software functions is within acceptable limits. Specific times when LPTs will be performed shall be prescribed in the verification specification.

2.3.4 Performance Operating Time and Failure-Free Performance Testing

One-thousand (1000) hours of operating/power-on time should be accumulated on all flight electronic hardware, and spares prior to launch.

In addition, at the conclusion of the performance verification program, payloads shall have demonstrated failure-free performance testing for at least the last 350 hours of operation. The demonstration may be conducted at the subsystem level of assembly when payload integration is accomplished at the launch site and the 350-hour demonstration cannot practicably be accomplished on the integrated payload. Failure-free operation during the thermal-vacuum test exposure is included as part of the demonstration with 100 hours of the trouble-free operation being logged at the hot-dwell temperatures and 100 hours being logged at the cold-dwell temperature. Major hardware changes during or after the verification program shall invalidate previous demonstration.

The general intent of the above requirements is to accumulate 1000 hours of operating time on all flight hardware, and to demonstrate trouble-free performance at high-, low-, and nominal temperature. However, it is understood that under certain conditions this goal may not be met. For example hardware change-out just prior to launch may not provide sufficient time to demonstrate these requirements. Also, the retest requirements following component failure during system level thermal vacuum, or other tests, must be evaluated on a case-by-case basis taking into account the criticality of the hardware element and the risk impact on achieving mission goals.

The guideline time requirements should be tailored up or down to reflect hardware classification, and mission duration.

2.3.5 Limited-Life Electrical Elements

A life test program shall be considered for electrical elements that have limited lifetimes. The verification plan shall address the life test program, identifying the electrical elements that require such testing, describing the test hardware that will be used, and the test methods that will be employed.